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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,548	12/27/2001	Shinji Saito	024016-00020	9580

7590                    04/19/2006

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[REDACTED] EXAMINER

LE, NHAN T

ART UNIT	PAPER NUMBER
	2618

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/026,548	SAITO, SHINJI	
	<b>Examiner</b>	<b>Art Unit</b>	
	Nhan T. Le	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 09 December 2005.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-28 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-3,5-11,17-26 and 28 is/are rejected.  
 7) Claim(s) 4,12-16 and 27 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                     | Paper No(s)/Mail Date. _____ .  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____ .                                  |

**DETAILED ACTION**

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/09/2005 has been entered.

**DETAILED ACTION*****Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1, 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bellaouar et al (US 6,308,049) in view of Honjo et al (US 6,622,010) further in view of Kasahara et al (US 6,714,772).

As to claim 1, Bellaouar teaches a PLL frequency synthesizer, comprising: a voltage-controlled oscillator (see fig. 5, number 6, col. 3, lines 64-67, col. 4, lines 1-26) for outputting an output frequency signal corresponding to a control voltage signal; a phase comparator (see fig. 5, number 3, col. 3, lines 64-67, col. 4, lines 1-26) for outputting an output signal corresponding to a phase comparison between the output

frequency signal and a reference frequency signal; and a charge pump circuit (see fig. 5, number 4, col. 3, lines 64-67, col. 4, lines 1-26) for varying the control voltage signal according to the phase-compared signal; whereby a feedback loop is configured, Bellaouar fails to teach a signal flow of the feedback loop is periodically varied in a predetermined period , the predetermined period including an output period of the reference frequency signal subjected to comparison in a phase comparison cycle of the phase comparator. Honjo teaches a signal flow of the feedback loop is periodically varied in a predetermined period, the predetermined period including an output period of the reference frequency signal subjected to comparison in a phase comparison cycle of the the phase comparator (see abstract col. 3, lines 6-67, col. 4, lines 1-8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Honjo into the system of Bellaouar in order to reduce the phase difference between the reference signal and the comparison signal (as suggested by Honjo col. 3, lines 61-67, col. 5, lines 63-67). The combination of Bellaouar and Honjo fails to teach wherein a feedback loop in a locked state is configured and the predetermined period including the timing of performing an operation of phase comparison between the output frequency signal and the reference signal in the phase comparator. Kasahara teaches wherein a feedback loop in a locked state is configured and the predetermined period including the timing of performing an operation of phase comparason between the output frequency signal and the reference signal in the phase comparator (see col. 8, lines 28-67, col. 9, lines 1-47). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made

to provide the teaching of Kasahara into the system of Bellaouar and Honjo in order to detect a flag in the phase of the feedback side pulse with the next rising time of the reference side pulse.

As to claim 21, the combination of Bellaour, Honjo and Kasahara teaches wherein the charge pump circuit includes an output capability switching circuit for selecting the capability of supply of an output signal outputted from the charge pump circuit (see Kasahara col. 6, lines 33-65).

As to claims 22-24, the combination of Bellaour, Honjo and Kasahara teaches wherein the output capability switching circuit selects a drive power source voltage for an output-stage circuit of the charge pump circuit, wherein the output capability switching circuit selects a drive current for an output-stage circuit of the charge pump circuit, wherein the output capability switching circuit selects an output transistor size for an output-stage circuit of the charge pump circuit (see Kasahara col. 6, lines 66-67, col. 7, lines 1-54).

As to claim 25, the claim is rejected as to claim 1.

As to claim 26, the combination of Bellaouar, Honjo and Kasahara teaches a frequency divider for frequency-dividing the reference frequency signal, and wherein a frequency signal compared in the phase comparator is a divided frequency signal outputted from the frequency divider (see fig. 5, number 7, col. 3, lines 64-67, col. 4, lines 1-26).

2. Claims 2, 3, 7, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bellaouar et al (US 6,308,049) in view of Honjo et al (US 6,622,010), Kasahara et al (US 6,714,772) further in view of Bortolini et al (US 5,473,640).

As to claim 2, the combination of Bellaouar, Honjo and Kasahara fails to teach the PLL frequency synthesizer, wherein the operation of the feedback loop periodically stops in the phase comparison cycle used in the phase comparator. Bortolini teaches the PLL wherein the operation of the feedback loop periodically stops in the phase comparison cycle used in the phase comparator through the switch operation (see fig. 1, number 13, col. 3, lines 1-50). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Bortolini into the system of Bellaouar, Honjo and Kasahara in order to provide signal control between the controller output and oscillator (as suggested by Bortolini, col. 3, lines 18-24).

As to claim 3, the combination of Bellaouar, Honjo, Kasahara and Bortolini also teach the feedback loop includes a loop opening/closing switch circuit therewithin (see Bortolini fig. 1, number 13, col. 3, lines 1-50).

As to claim 7, the combination of Bellaouar, Honjo, Kasahara and Bortolini teaches the PLL, wherein the feedback loop stops the output of an output signal from the charge pump circuit (see Bortolini fig. 1, number 13, col. 3, lines 1-50).

As to claim 8, the combination of Bellaouar, Honjo, Kasahara and Bortolini also discloses the PLL frequency synthesizer, wherein the charge pump circuit includes a

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path opening/closing switch circuit in an output path for an output signal outputted from the charge pump circuit (see Bortolini see fig. 1, number 13, col. 3, lines 1-50).

3. Claims 5, 6, 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bellaouar et al (US 6,308,049) in view of Honjo et al (US 6,622,010), Kasahara et al (US 6,714,772), Bortolini et al (US 5,473,640) further in view of Weindorf (US 6,396,217).

As to claims 5, 6, the combination of Bellaouar, Honjo, Kasahara and Bortolini fails to teach the loop opening/closing switch circuit includes an MOS transistor or JFET transistor. Weindorf teaches the loop opening/closing switch circuit includes an MOS transistor or JFET transistor (see fig. 3, number 326, col. 7, lines 46-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Weindorf into the system of Bellaouar, Honjo, and Bortolini because MOS and JFET transistor switches have advantages such as high switching speed.

As to claims 9, 10, the claims are rejected for the same reason as stated in claims 5, 6 above.

4. Claims 11, 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bellaouar et al (US 6,308,049) in view of Honjo et al (US 6,622,010), Kasahara et al (US 6,714,772) further in view of Abe et al (US 5,794,130).

As to claim 11, the combination of Bellaouar, Honjo and Kasahara teaches the PLL frequency synthesizer, wherein at least one filter circuit for determining the signal flow of the feedback loop is provided in a path which extends from the charge pump

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circuit to the voltage-controlled oscillator. However, the combination of Bellaouar, Honjo and Kasahara fails to teach the filtering characteristic of the filter circuit is periodically varied in the phase comparison cycle of the phase comparator. Abe teaches a synthesizer including PLL and variable time constant filter (see col. 2, lines 3-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Abe into the system of Bellaouar, Honjo and Kasahara in order to suppress sudden fluctuations in the output level from the filters when time constant is switched (as suggested by Abe at col. 2, lines 22-24).

As to claims 17, 18 the claim is rejected for the same reason as stated in claim 11 above.

5. Claims 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bellaouar et al (US 6,308,049) in view of Honjo et al (US 6,622,010), Kasahara et al (US 6,714,772), Abe et al (US 5,794,130) and in further view of Weindorf (US 6,396,217).

As to claims 19, 20, the combination of Bellaouar, Honjo, Kasahara and Abe fails to teach the resistive element device is an MOS transistor or JFET transistor. Weindorf teaches an MOS transistor or JFET transistor (see fig. 3, number 326, col. 7, lines 46-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Weindorf into the system of Bellaouar, Honjo, Kasahra and Abe because MOS and JFET transistor switches have advantages such as high switching speed.

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bellaouar et al (US 6,308,049) in view of Honjo et al (US 6,622,010), Kasahara et al (US 6,714,772), Abe et al (US 5,794,130) and in further view of Mole et al (US 6,226,509).

As to claim 28, the combination of Bellaouar, Honjo, Kasahara and Abe fails to teach that the filter circuit is a voltage-driven type. Mole teaches the filter circuit is a voltage-driven type (see col. 10, lines 33-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Nishikawa into the system of Bellaouar, Honjo, Kasahara and Abe so that the cost can be reduced since there is no extra component is required in the integration of the filter (as suggested by Mole, see col. 10, lines 33-41).

#### ***Allowable Subject Matter***

Claims 4, 12-16, 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claim 4, the applied reference fails to teach the PLL frequency synthesizer wherein a first filter circuit and a second filter circuit for determining the signal flow of the feedback loop are provided in a path which extends from the charge pump circuit to the voltage-controlled oscillator, and the loop opening/closing switch circuit is provided between the first filter circuit and the second filter circuit as cited in the claim.

As to claim 12, the applied reference fails to teach the PLL frequency synthesizer , wherein the filter circuit includes, a bypass path group having at least two bypass

paths different in filter characteristic, and a selector switch circuit which selects a predetermined bypass path from the bypass path group as specified in the claim.

***Response to Arguments***

Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T Le whose telephone number is 571-272-7892. The examiner can normally be reached on 08:00-05:00 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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4-16-2006

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